

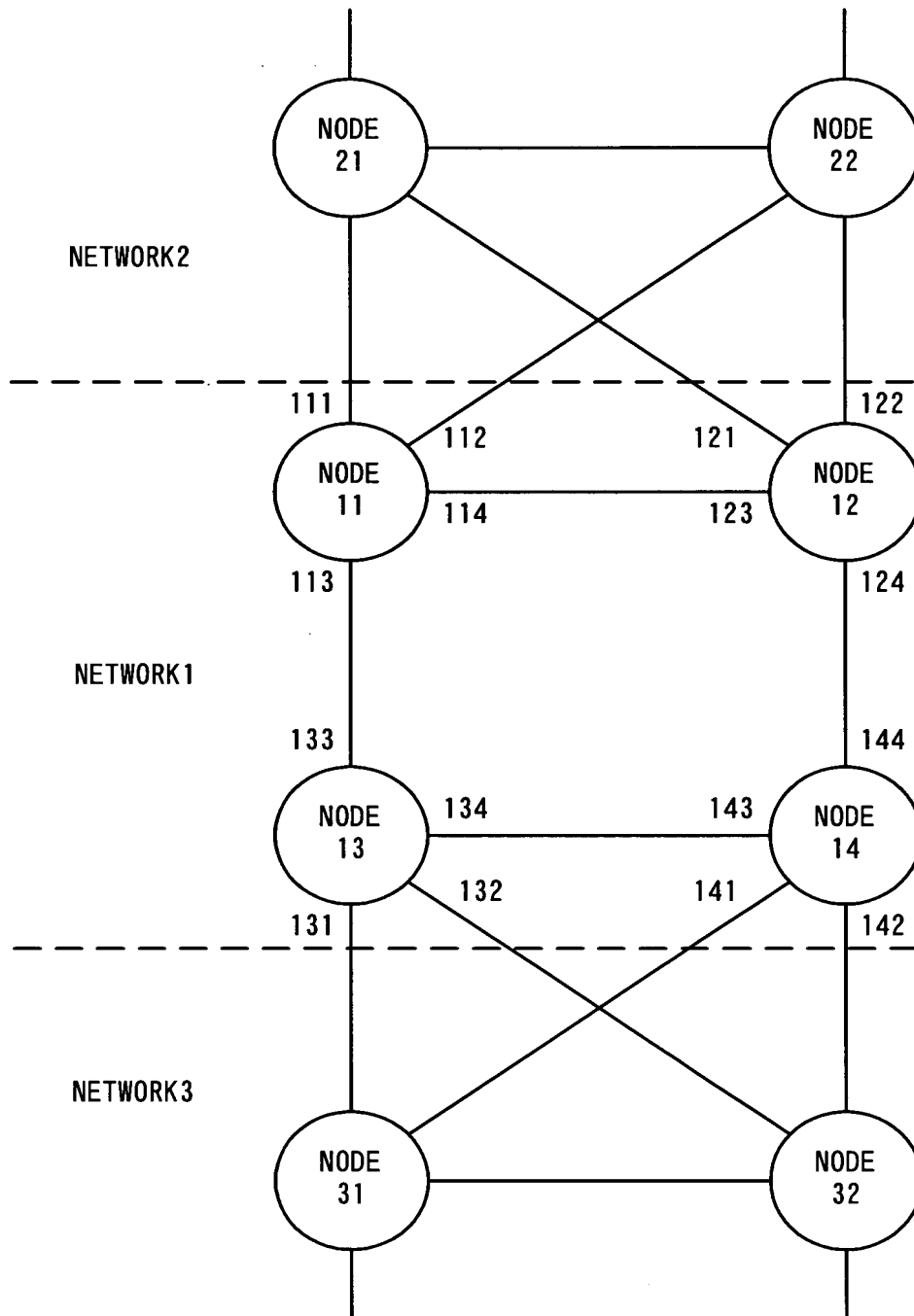
FIG. 1

FIG 2

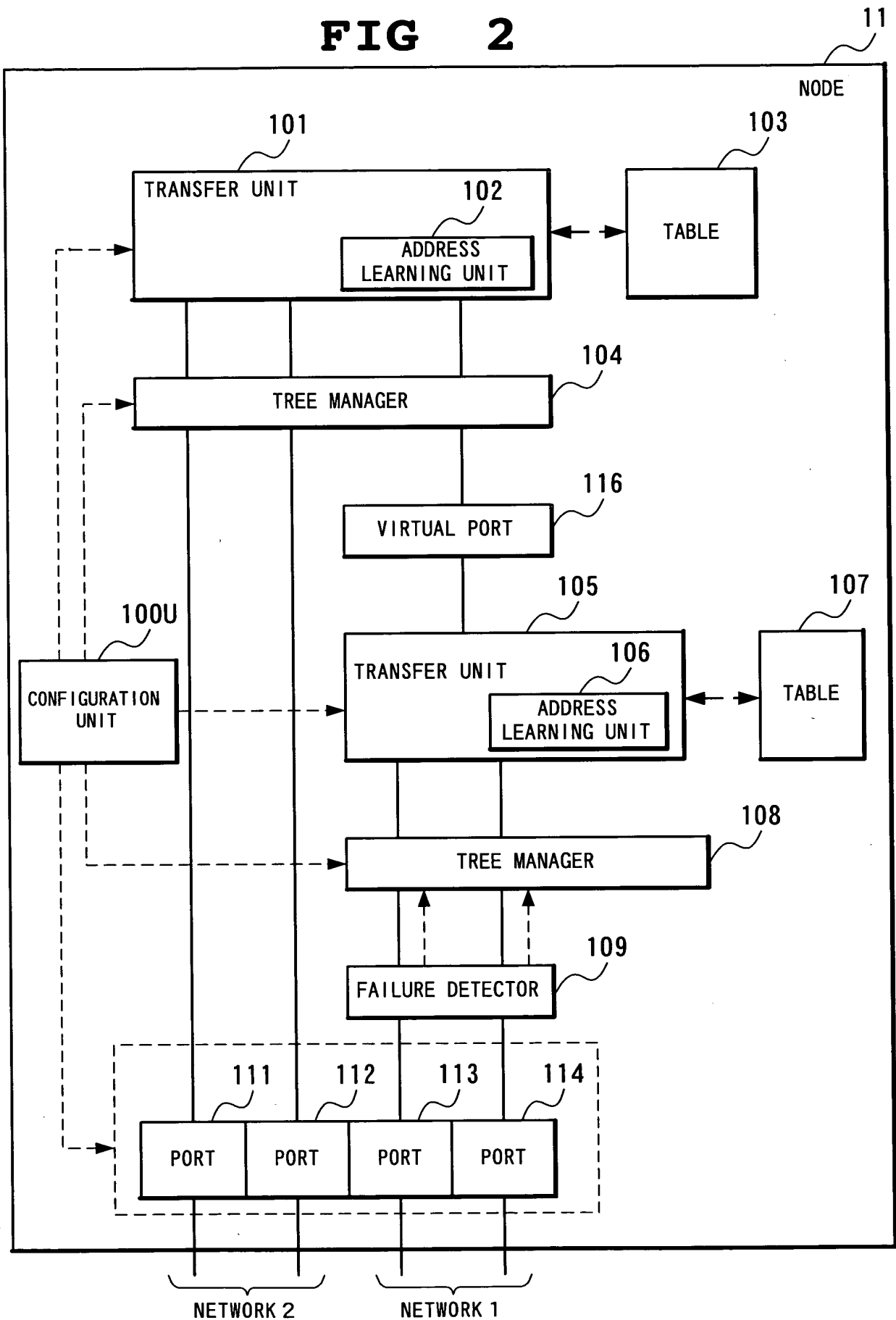


FIG. 3

103

1031 DESTINATION MAC	1032 OUTPUT PORT
1A 12 26 4F 5G 08	111
30 34 7D 5B E8 FF	116
58 DC FE 32 11 9A	116
BB 7C 67 28 09 12	112

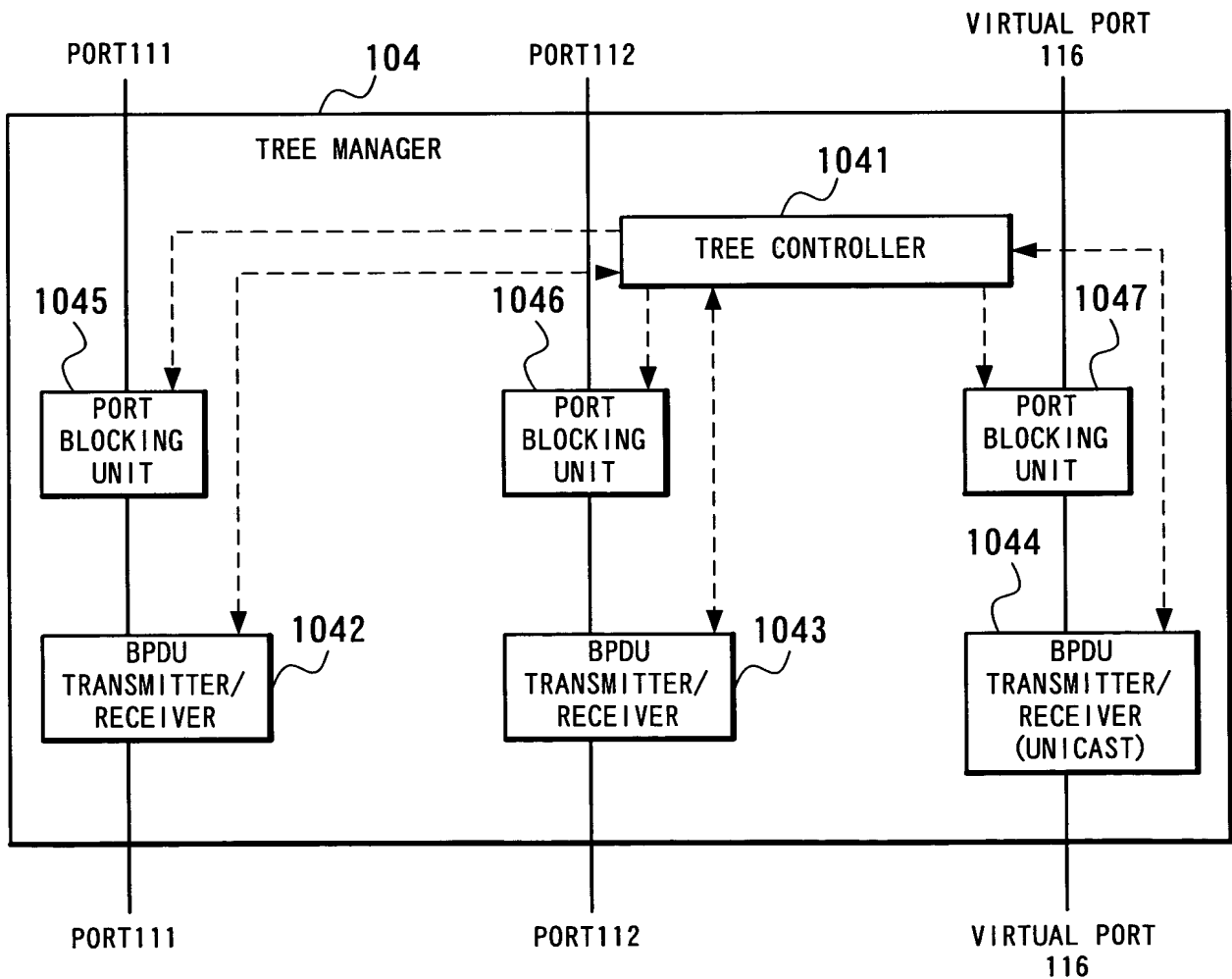
FIG. 4

FIG. 5

107

DESTINATION MAC	OUTPUT PORT
1A 12 26 4F 5G 08	111
30 34 7D 5B E8 FF	113
58 DC FE 32 11 9A	114
BB 7C 67 28 09 12	116

1071

1072

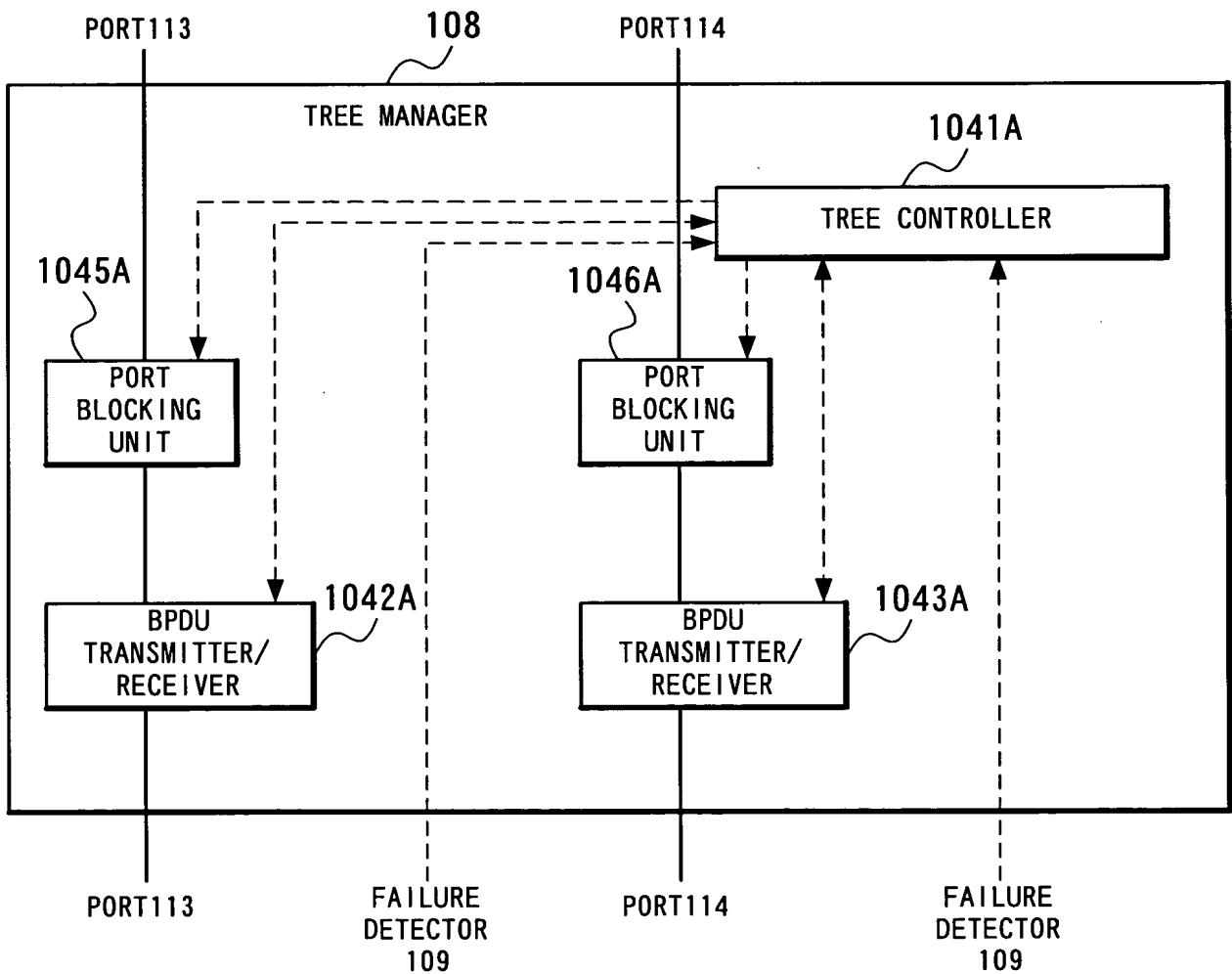
FIG. 6

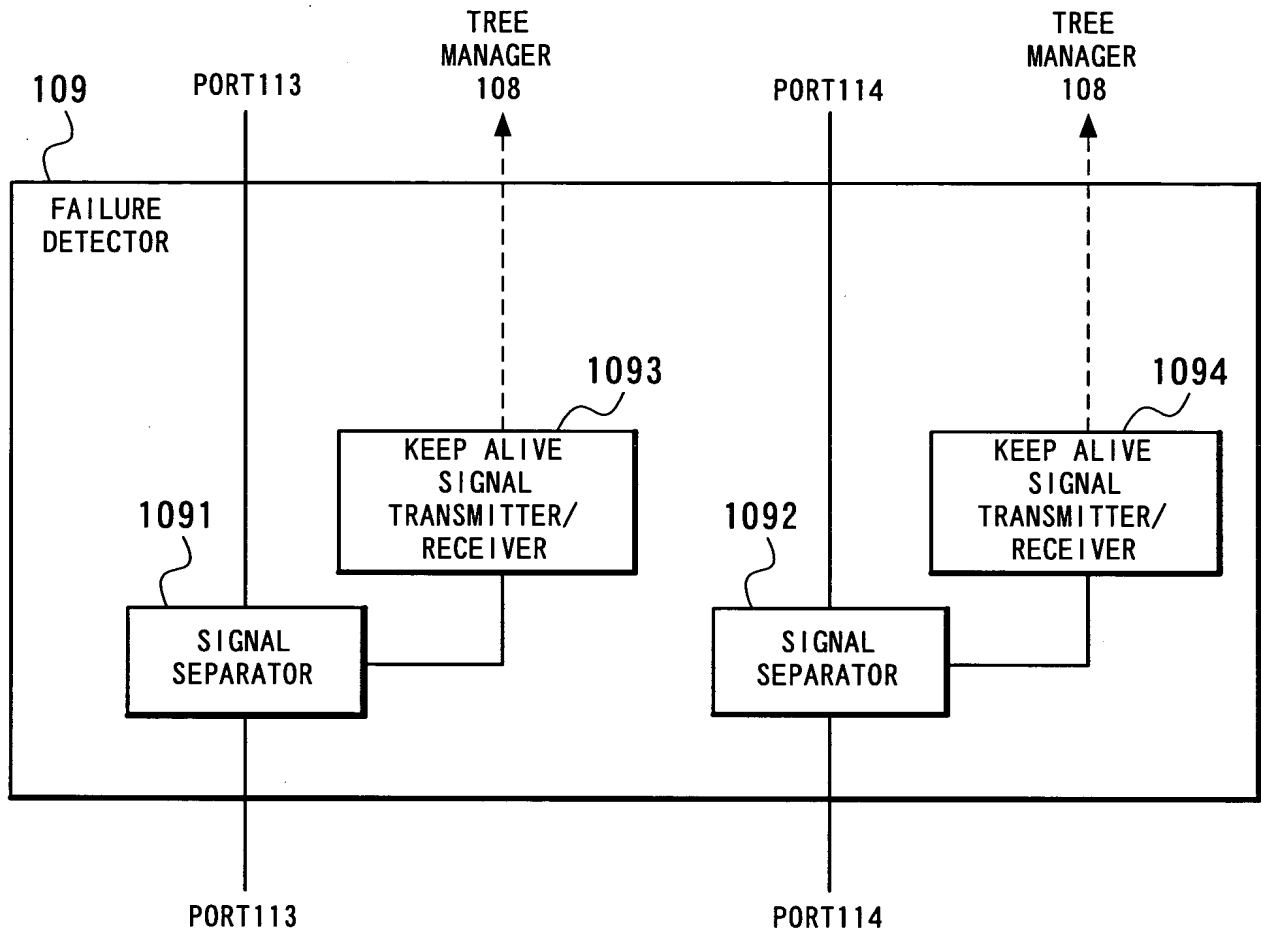
FIG 7

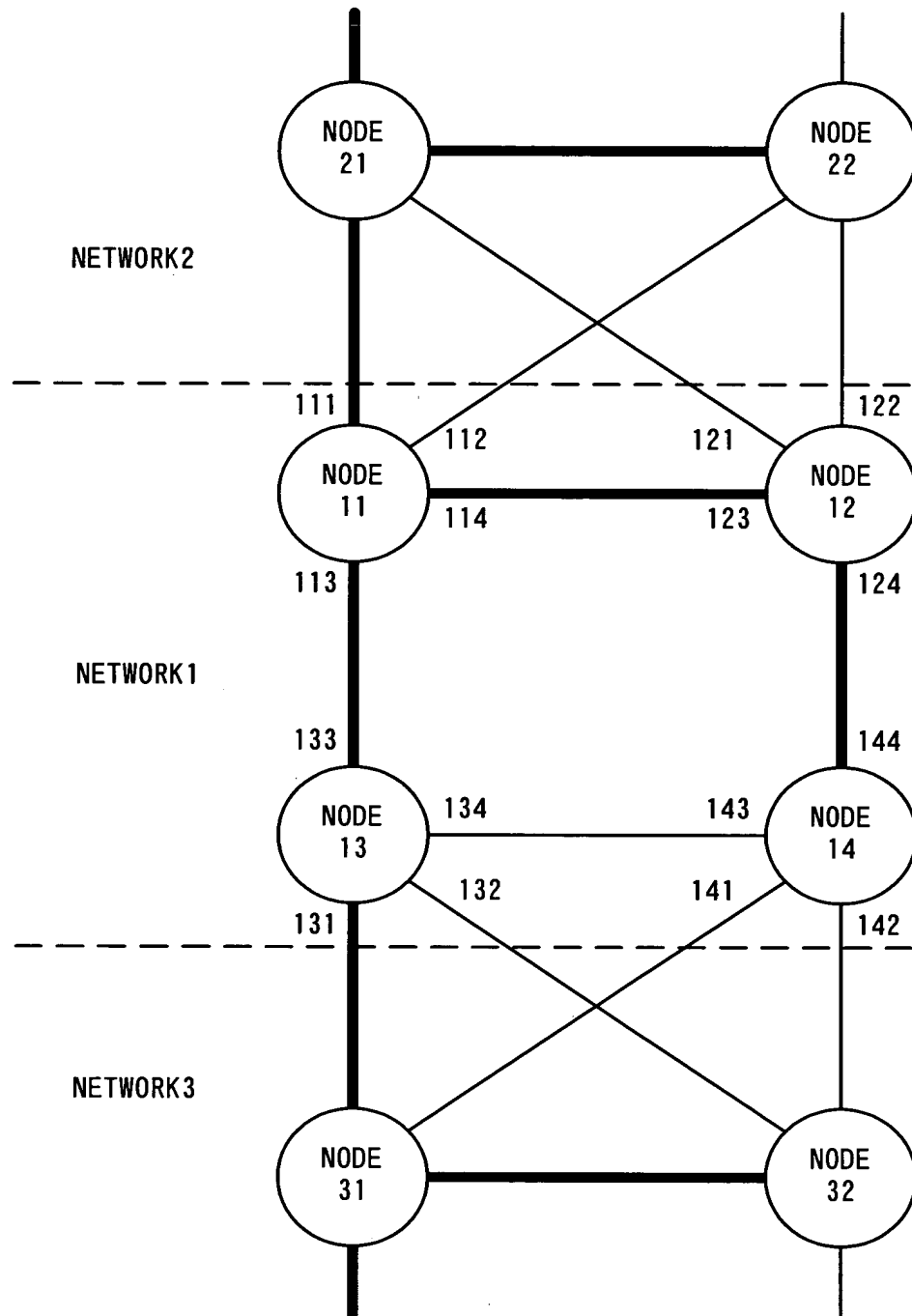
FIG. 8

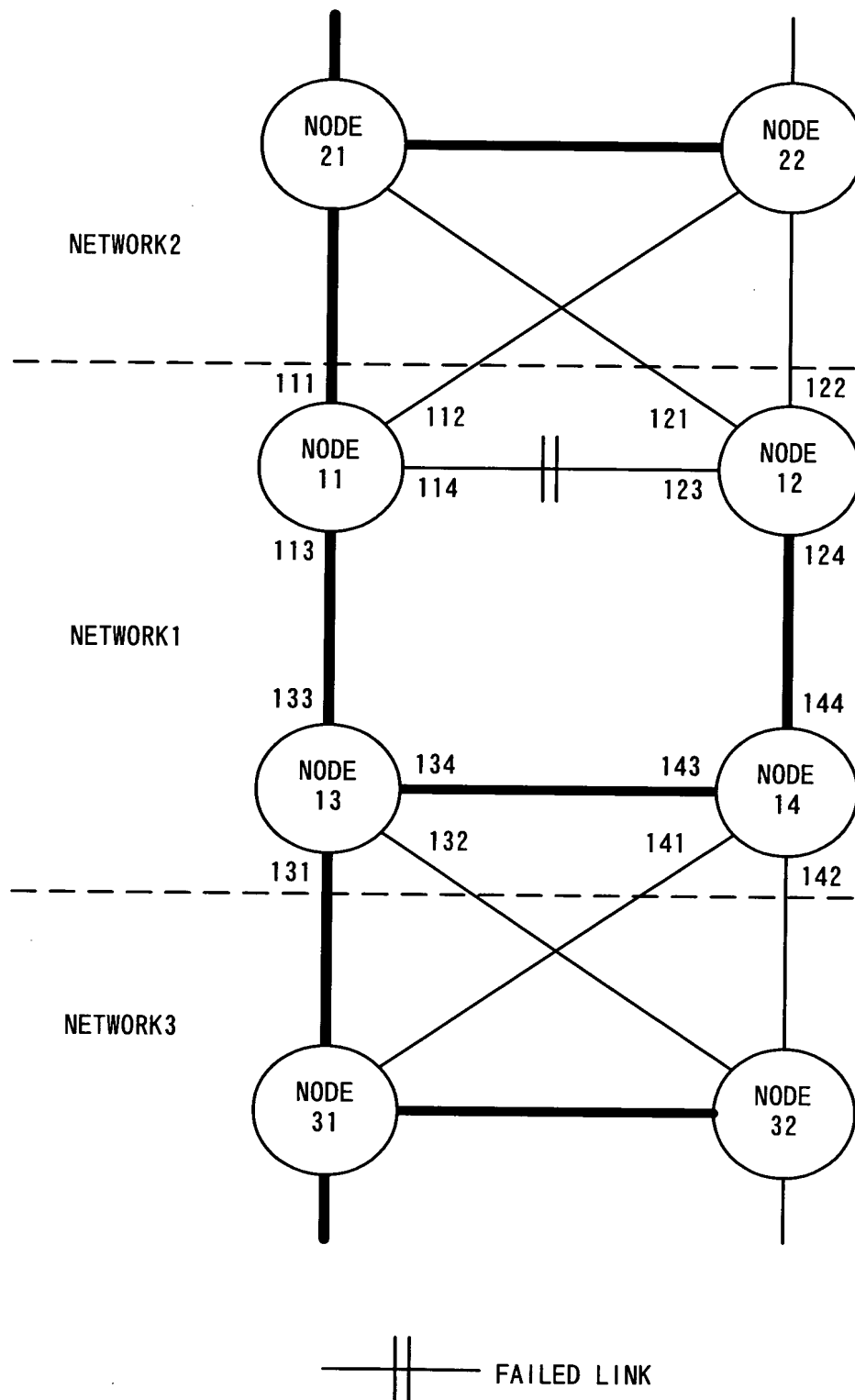
FIG 9

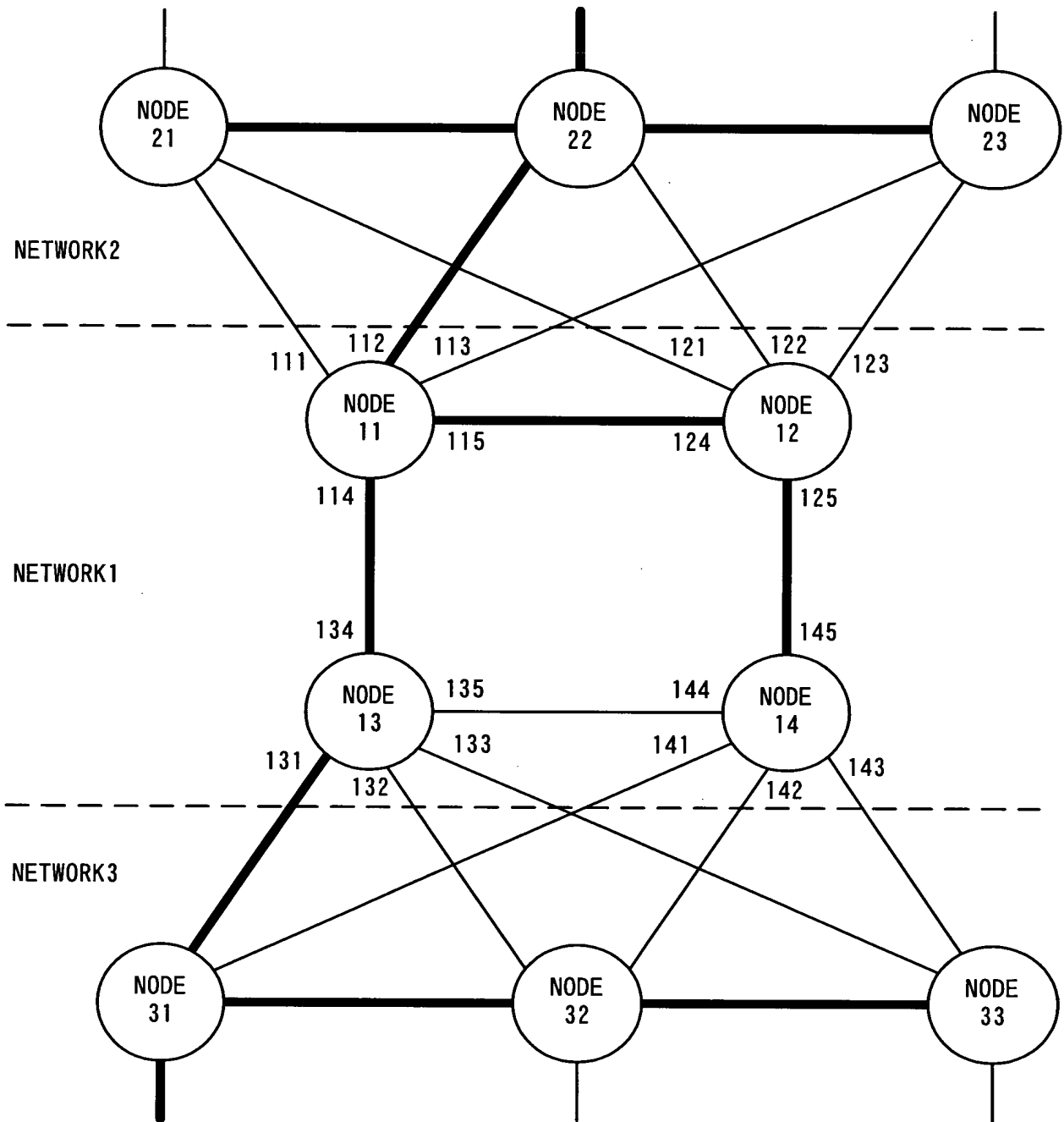
FIG. 10

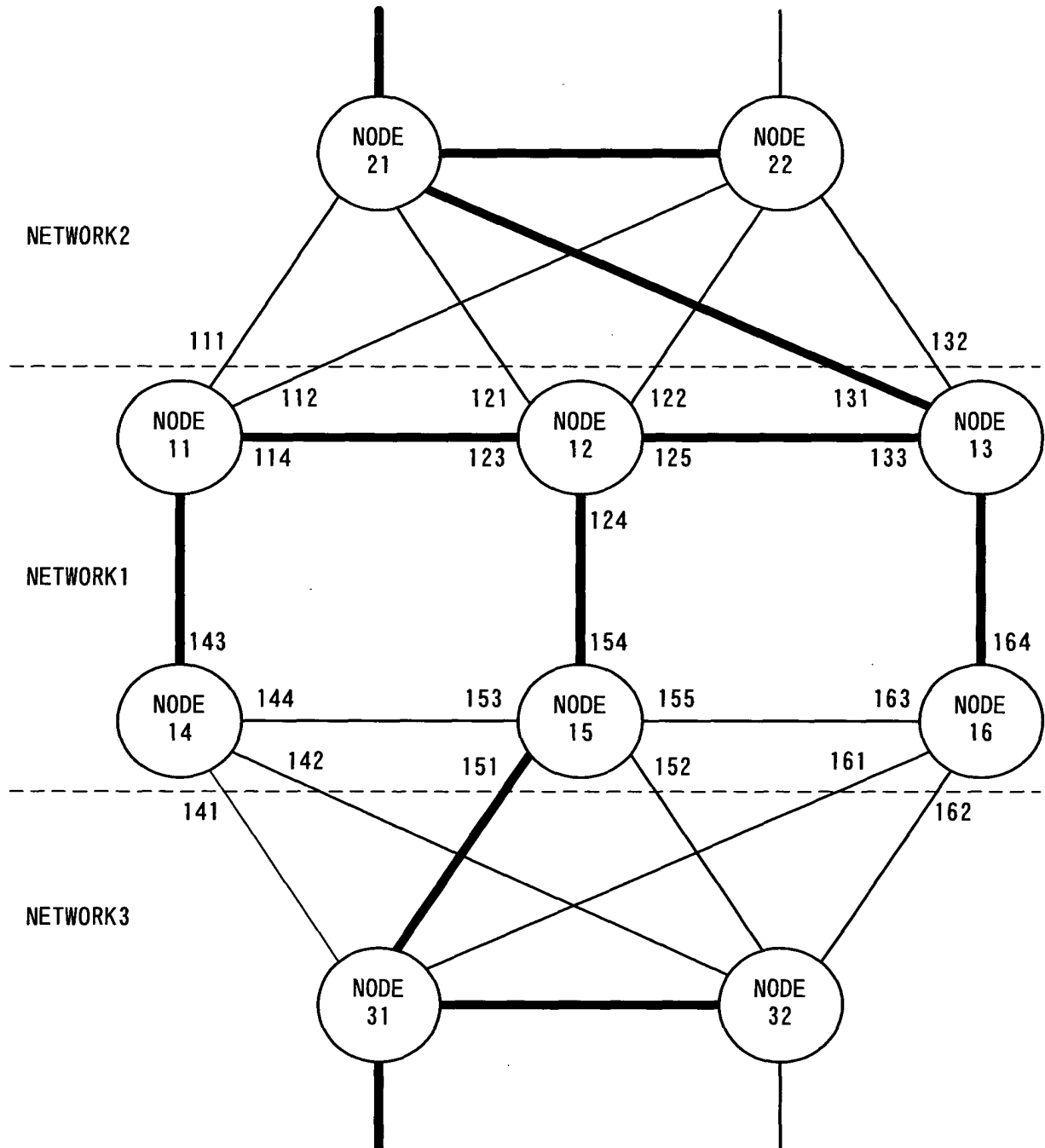
FIG. 11

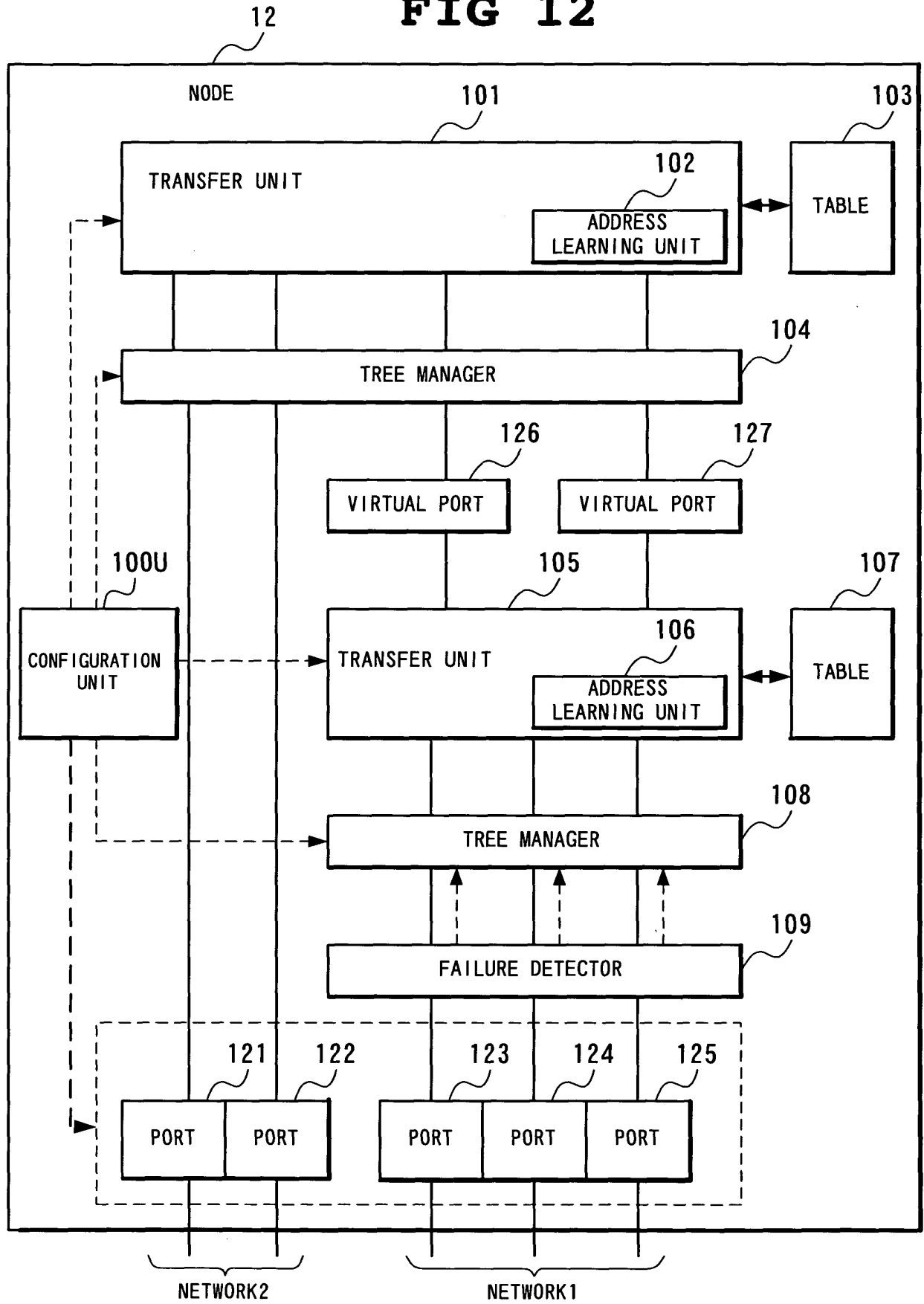
FIG 12

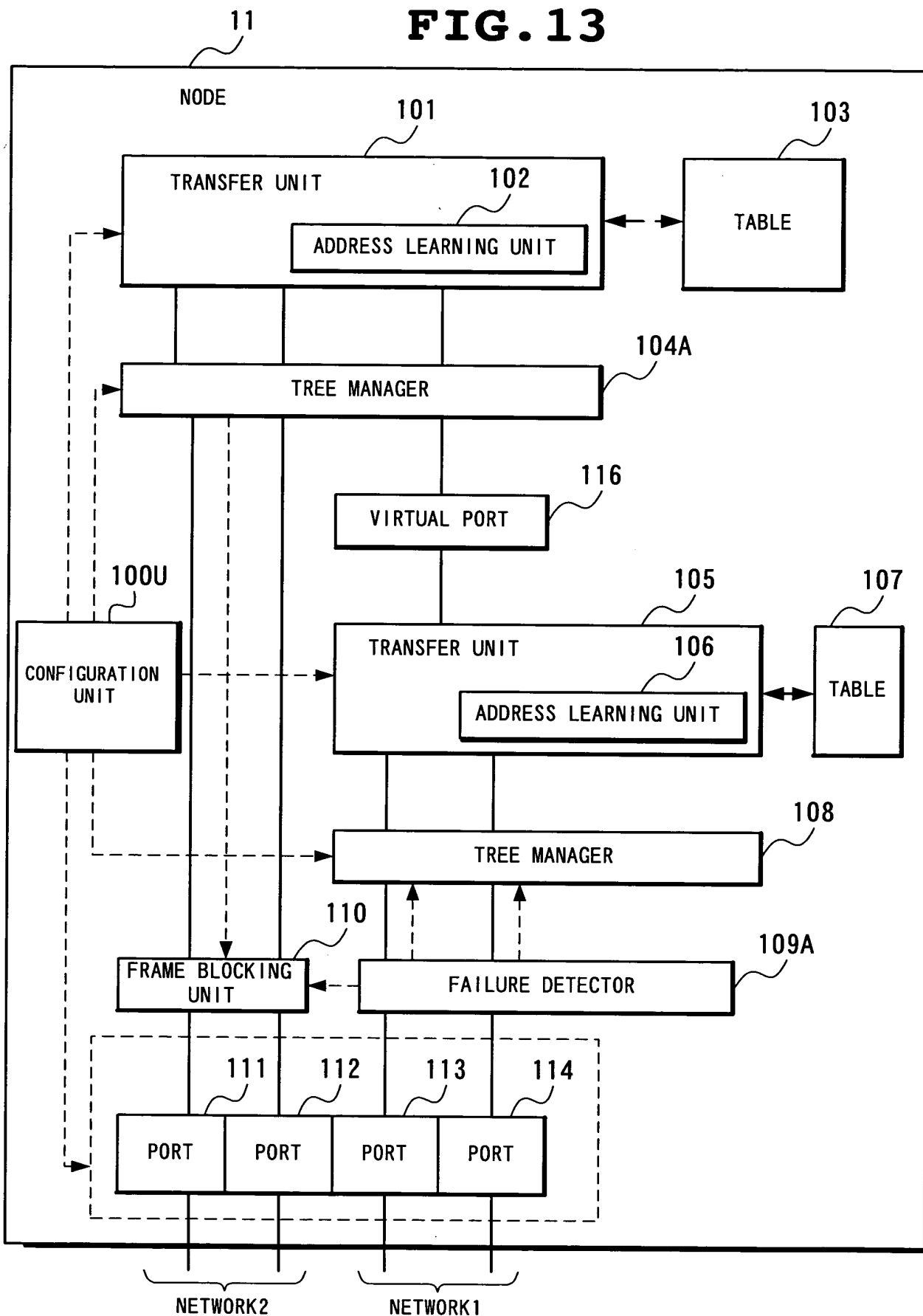
FIG. 13

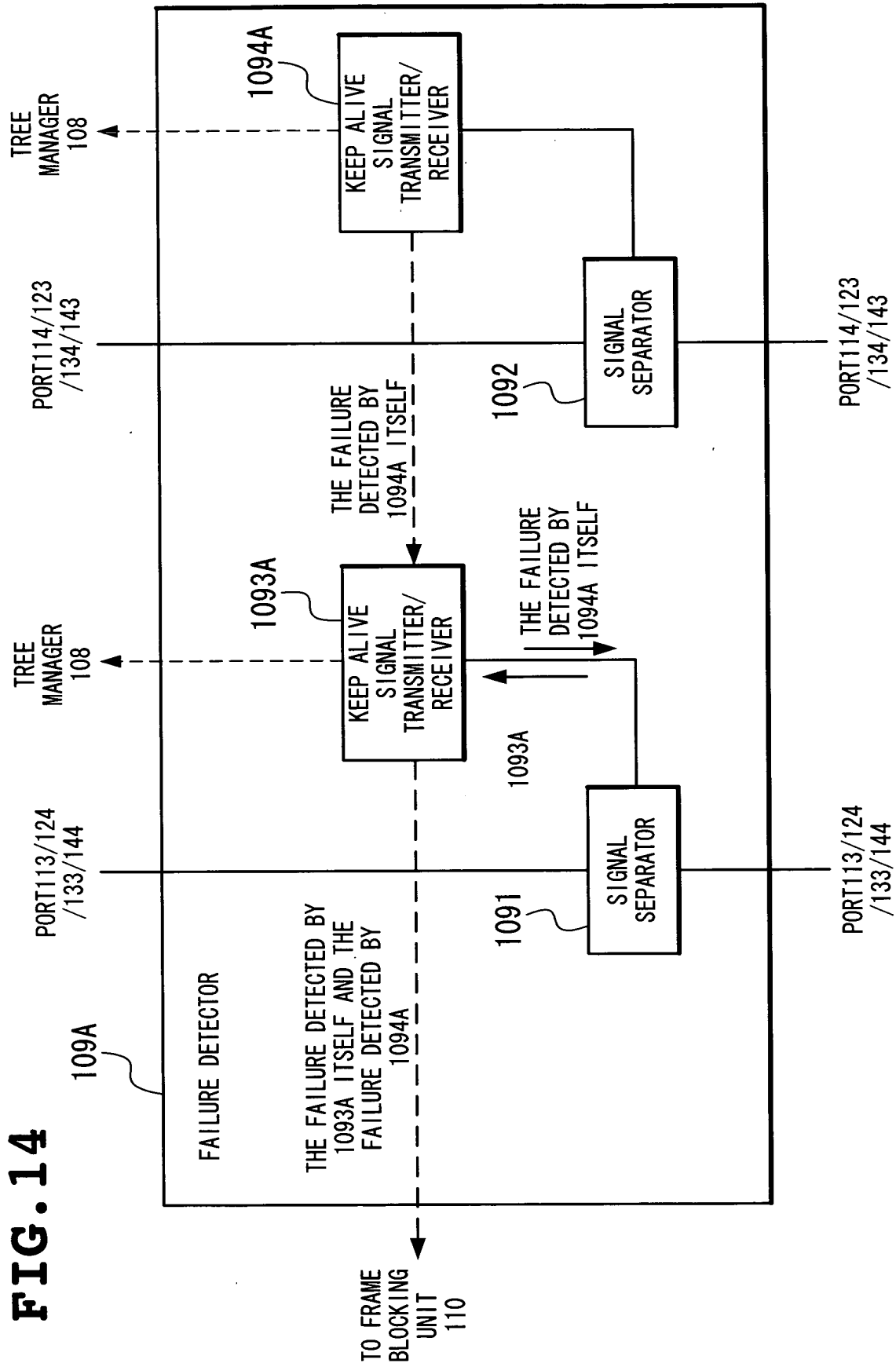
FIG. 14

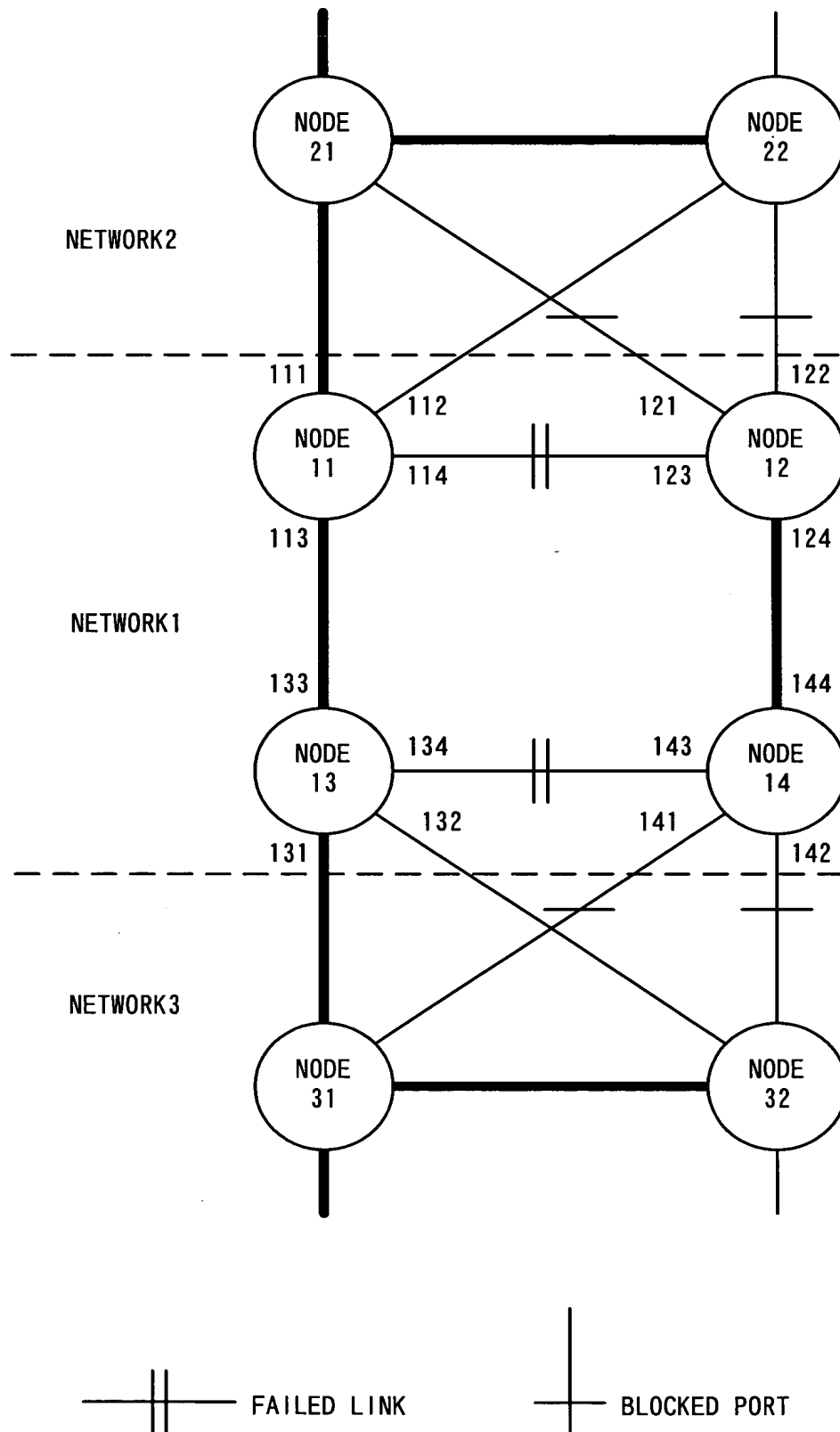
FIG. 15

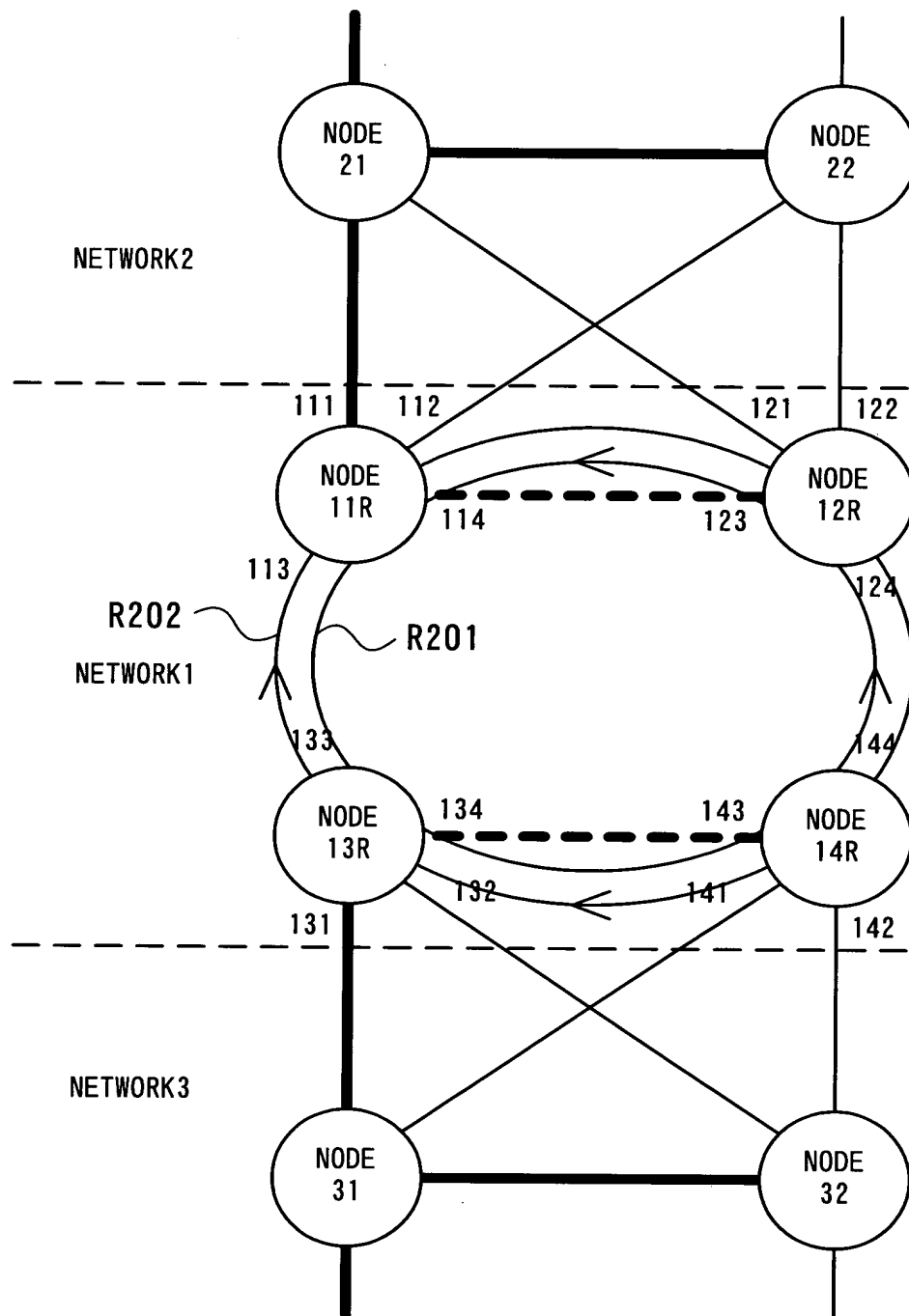
FIG. 16

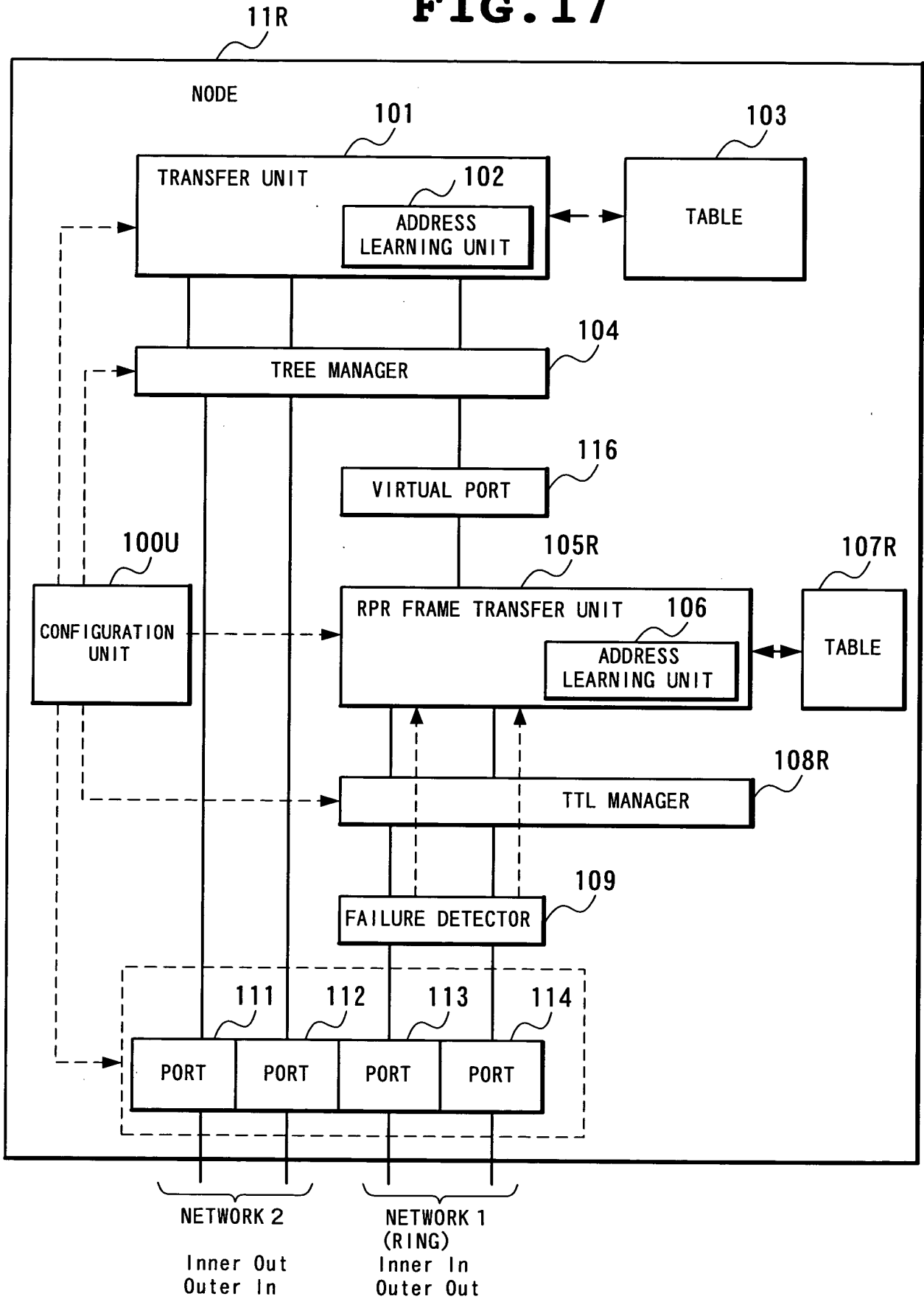
FIG. 17

FIG. 18

107R

1071

1071R

1072R

1072

DESTINATION MAC	DESTINATION RPR NODE	RING ID	OUTPUT PORT	
01 80 C2 00 00 00	1 2 R	Outer	1 1 4	PREVIOUSLY SET
30 34 7D 5B E8 FF	1 3 R	Inner	1 1 3	EXAMPLE
58 DC FE 32 11 9A	1 2 R	Outer	1 1 4	EXAMPLE
BB 7C 67 28 09 12	1 1 R	DELETE	1 1 6	EXAMPLE

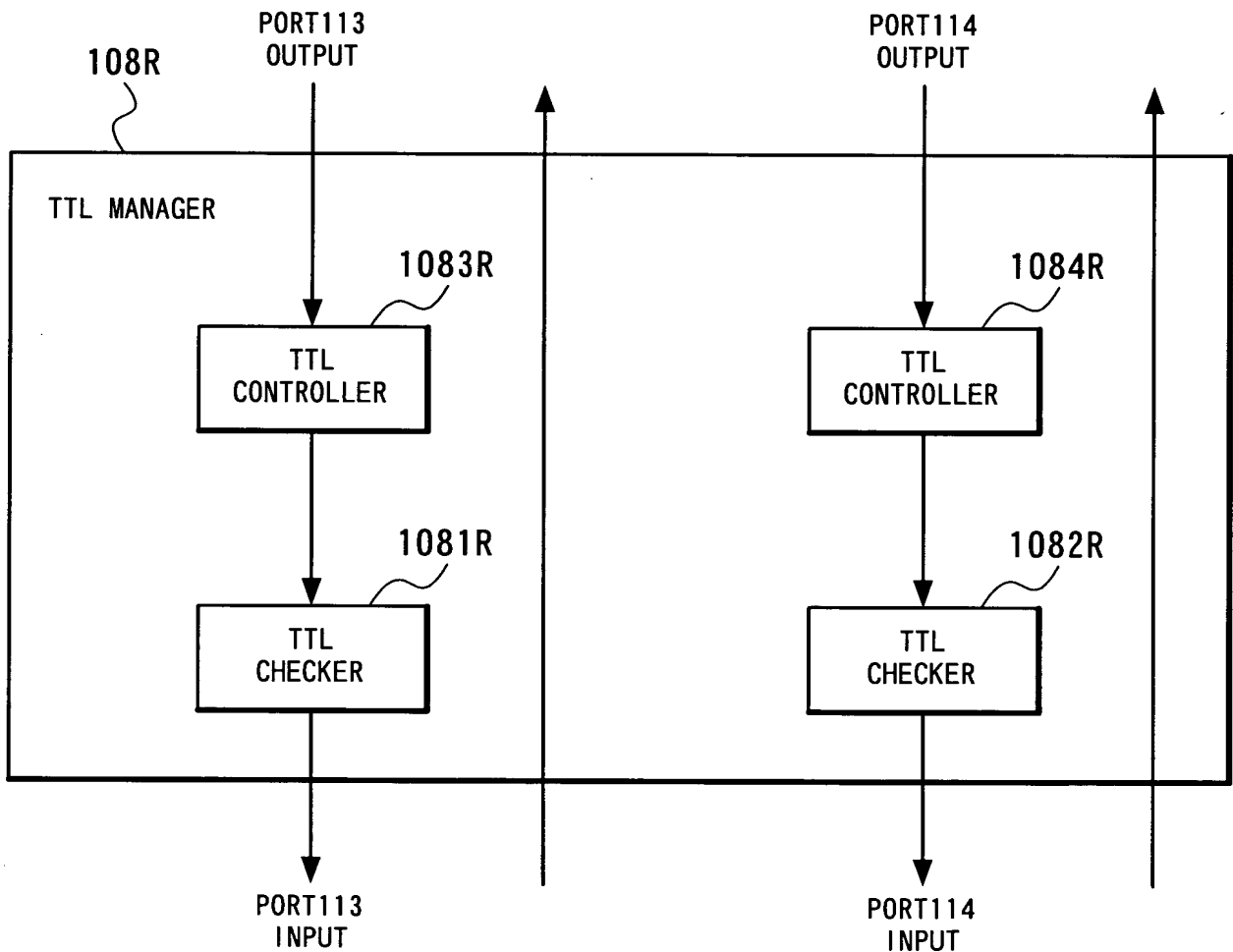
FIG. 19

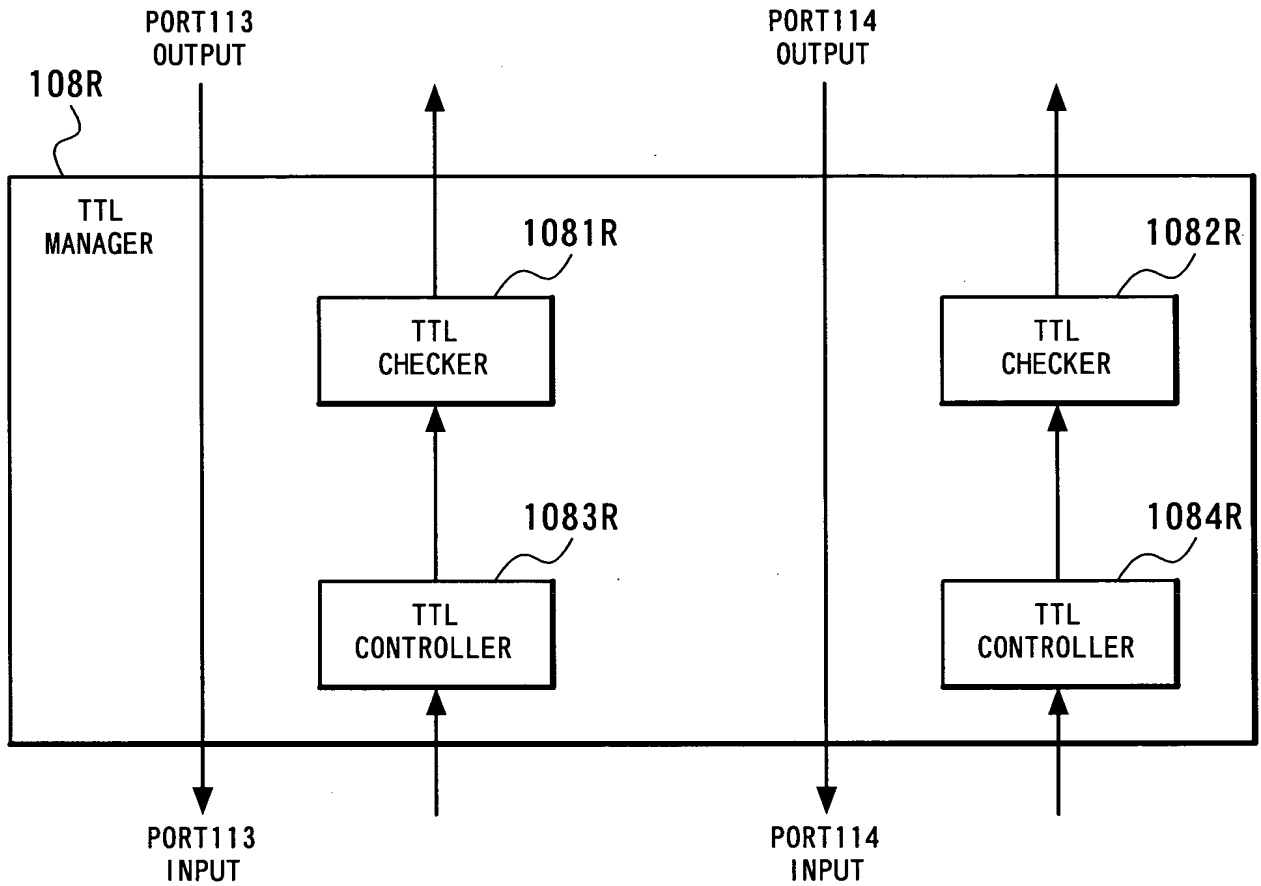
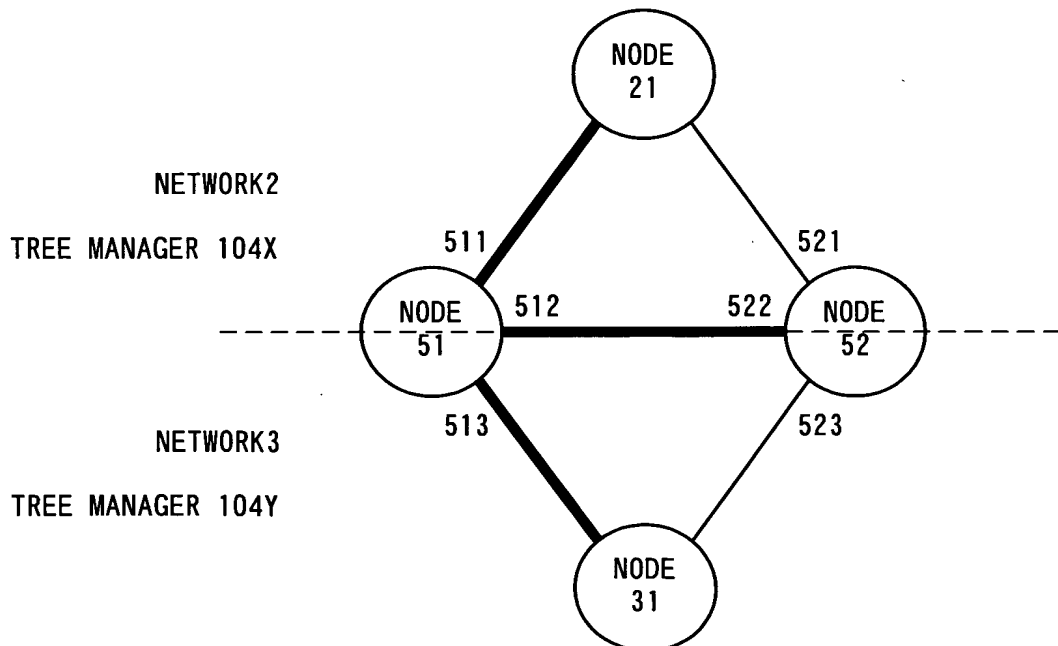
FIG 20**FIG. 21**

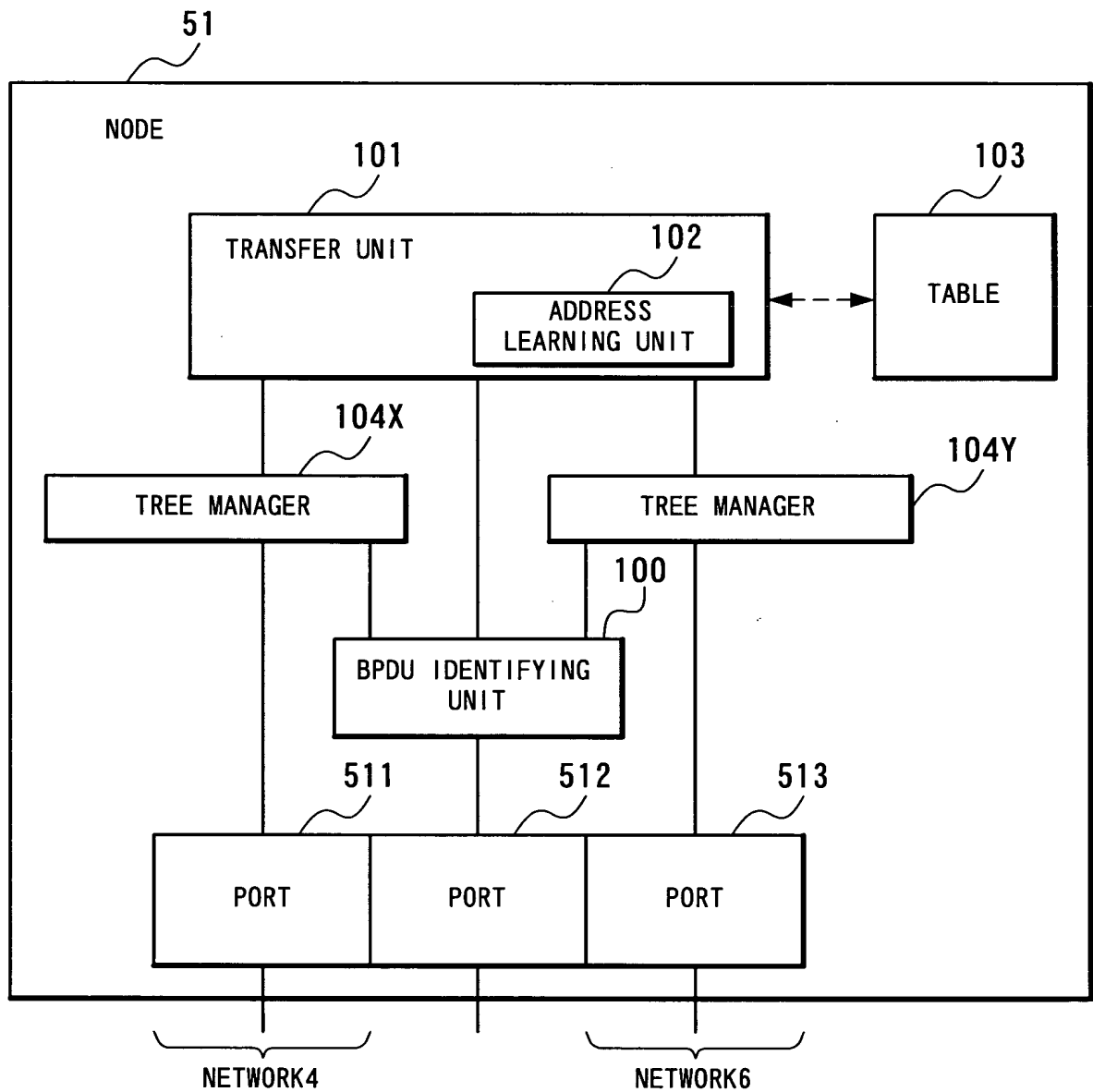
FIG. 22

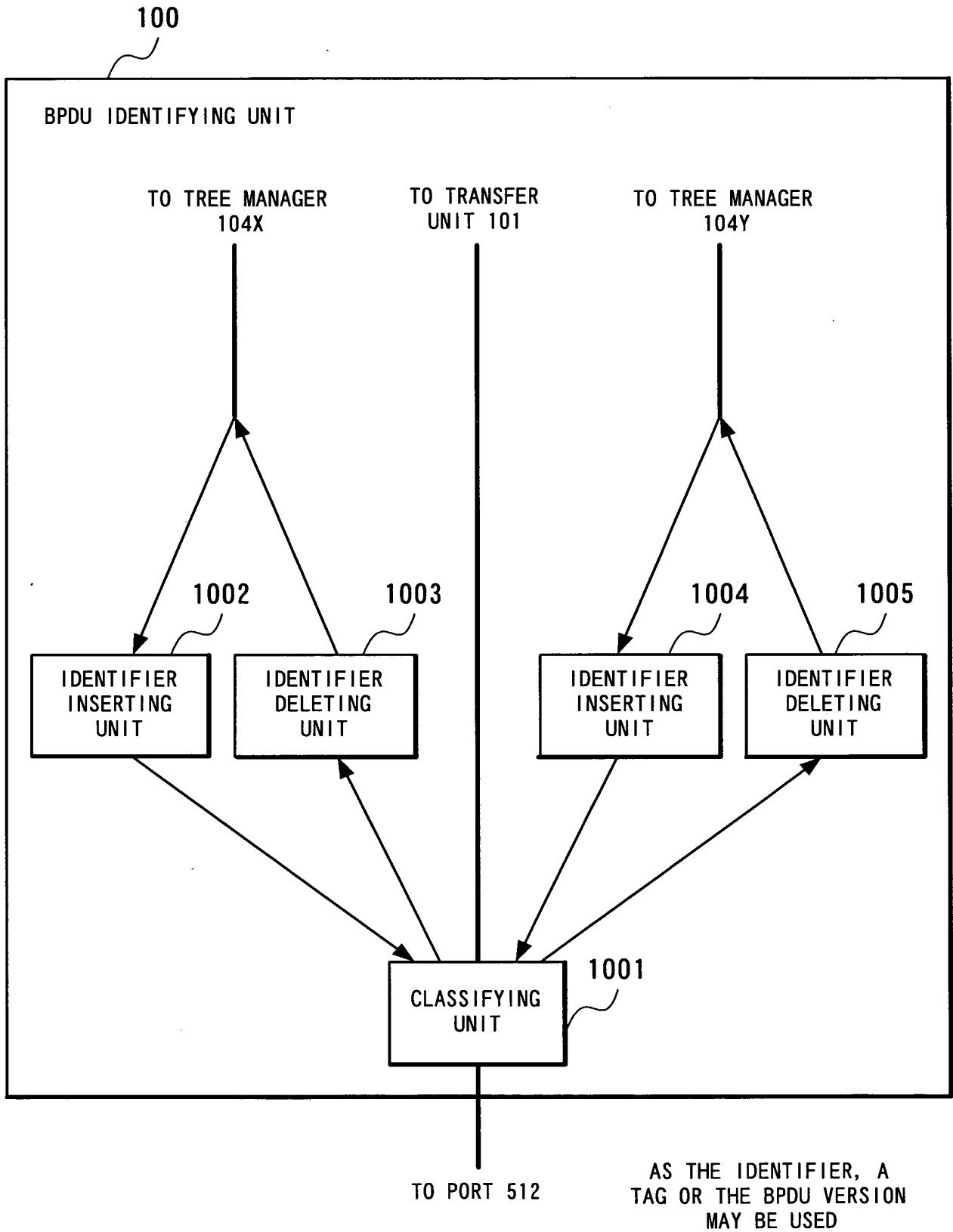
FIG. 23

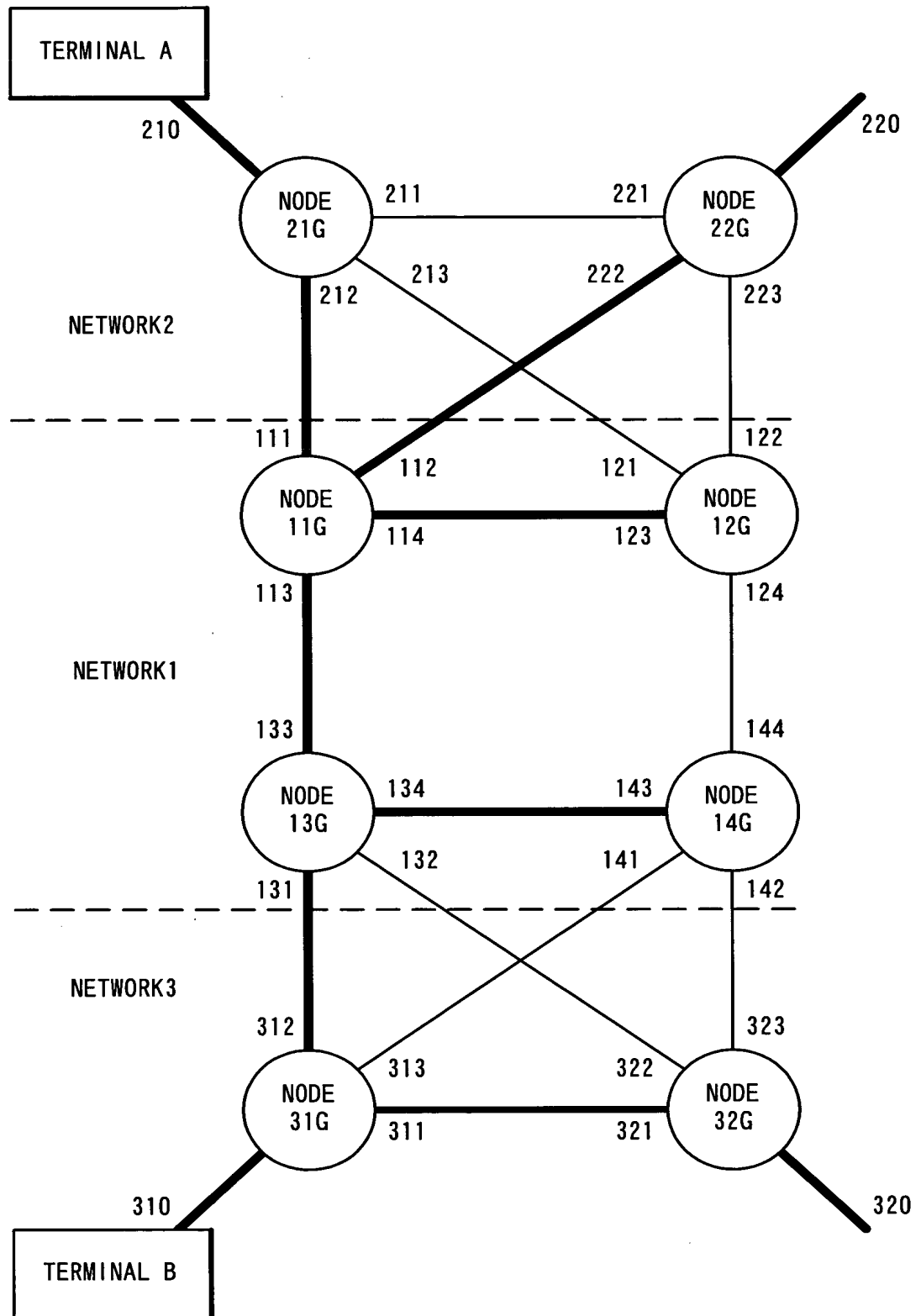
FIG. 24

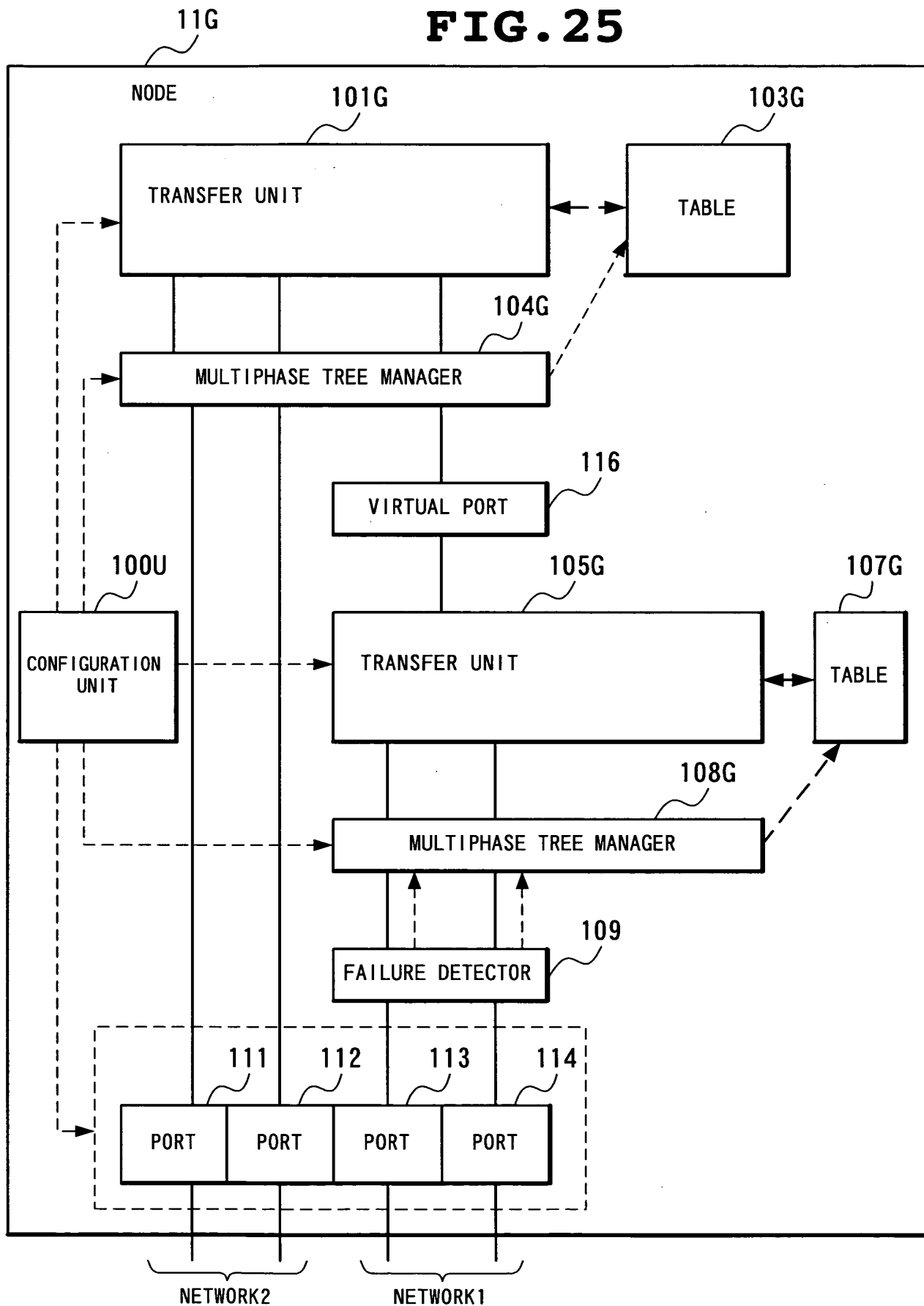
FIG. 25

FIG. 26

DESTINATION IDENTIFIER TAG	OUTPUT PORT
0 0 0 0	1 1 1
0 0 3 1	1 1 6
0 1 5 6	1 1 6
4 0 9 5	1 1 2

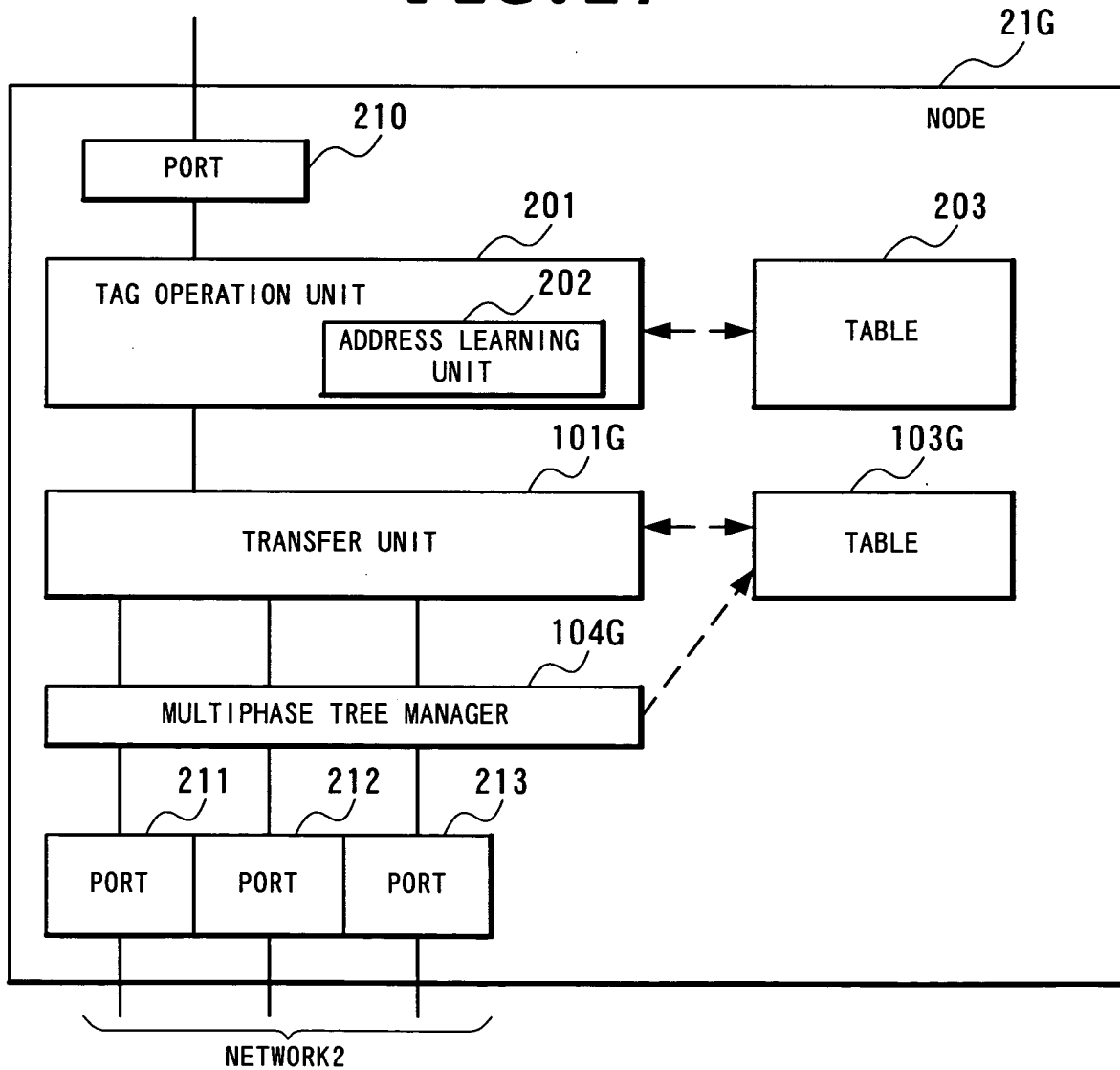
FIG. 27

FIG. 28

203

2301

2302

DESTINATION MAC	INSERTION TAG
1A 12 26 4F 5G 08	0 0 0 0
22 00 00 00 00 22	0 0 3 1
58 DC FE 32 11 9A	1 8 6 2
BB 7C 67 28 09 12	4 0 9 5

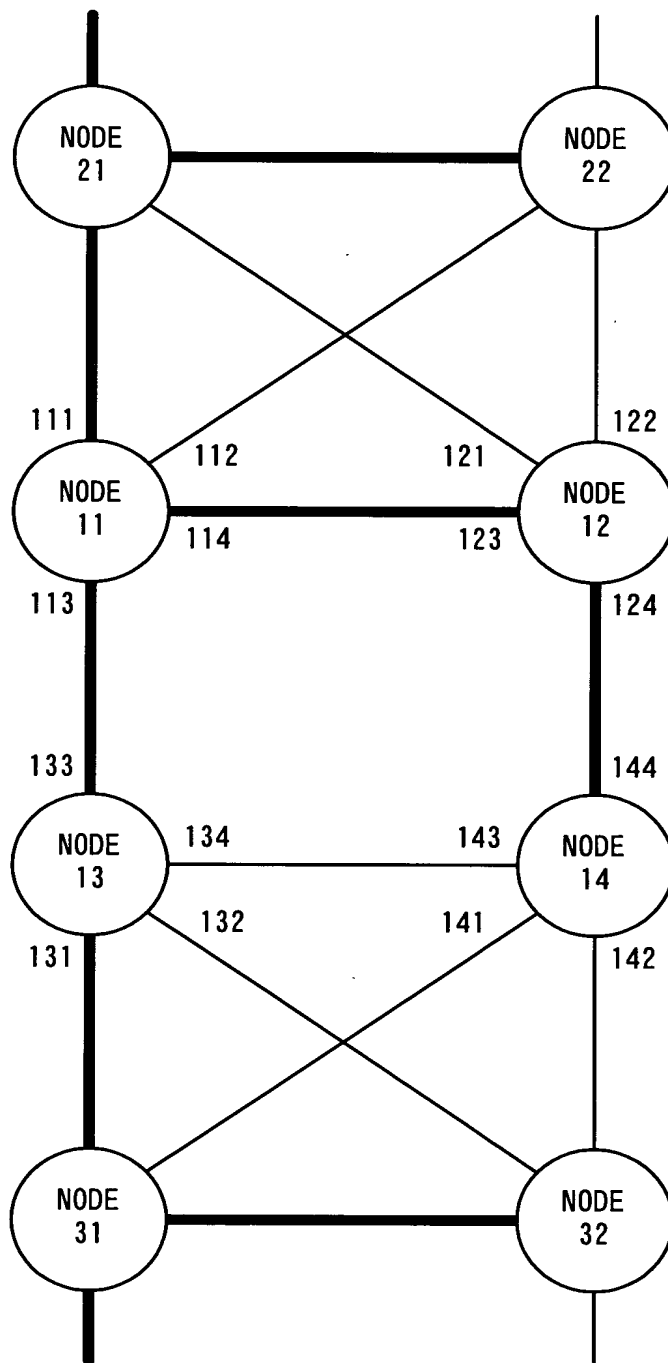
FIG. 29

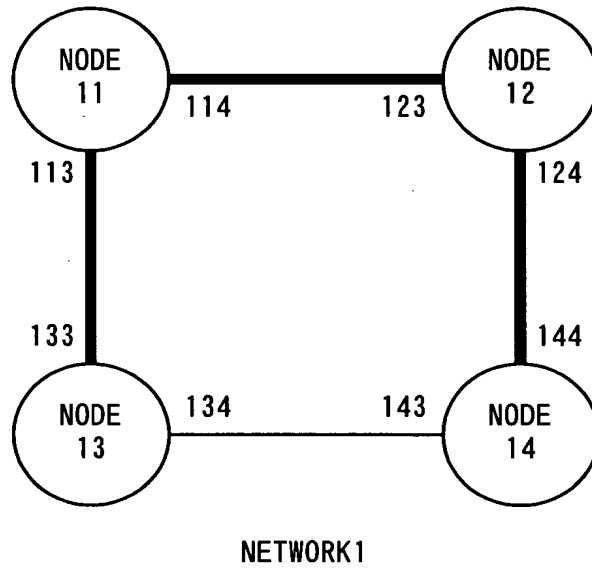
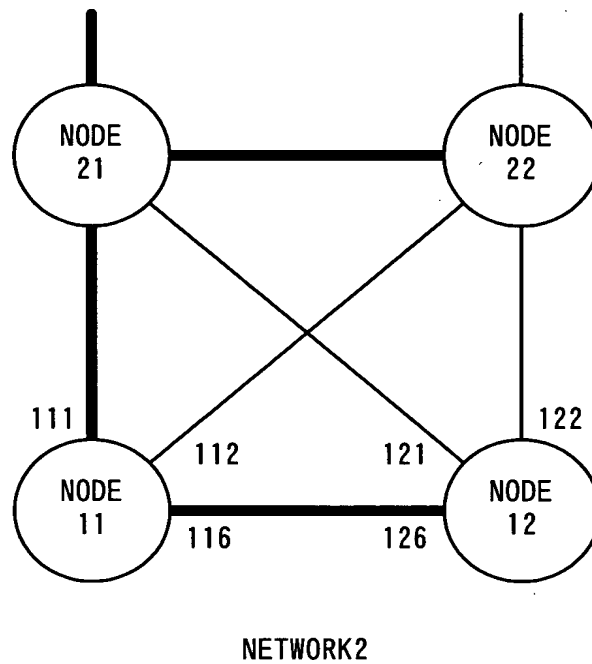
FIG. 30A**FIG. 30B**

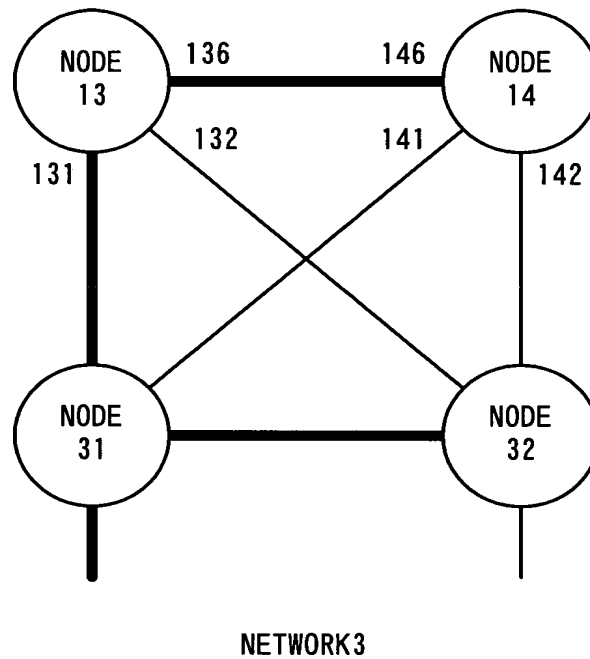
FIG. 30C

FIG. 31

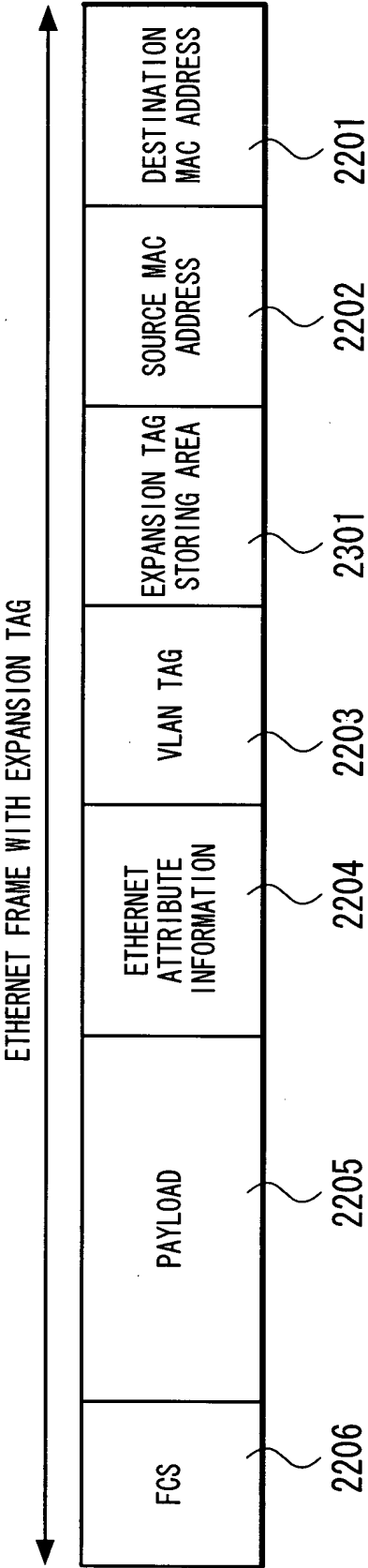


FIG. 32

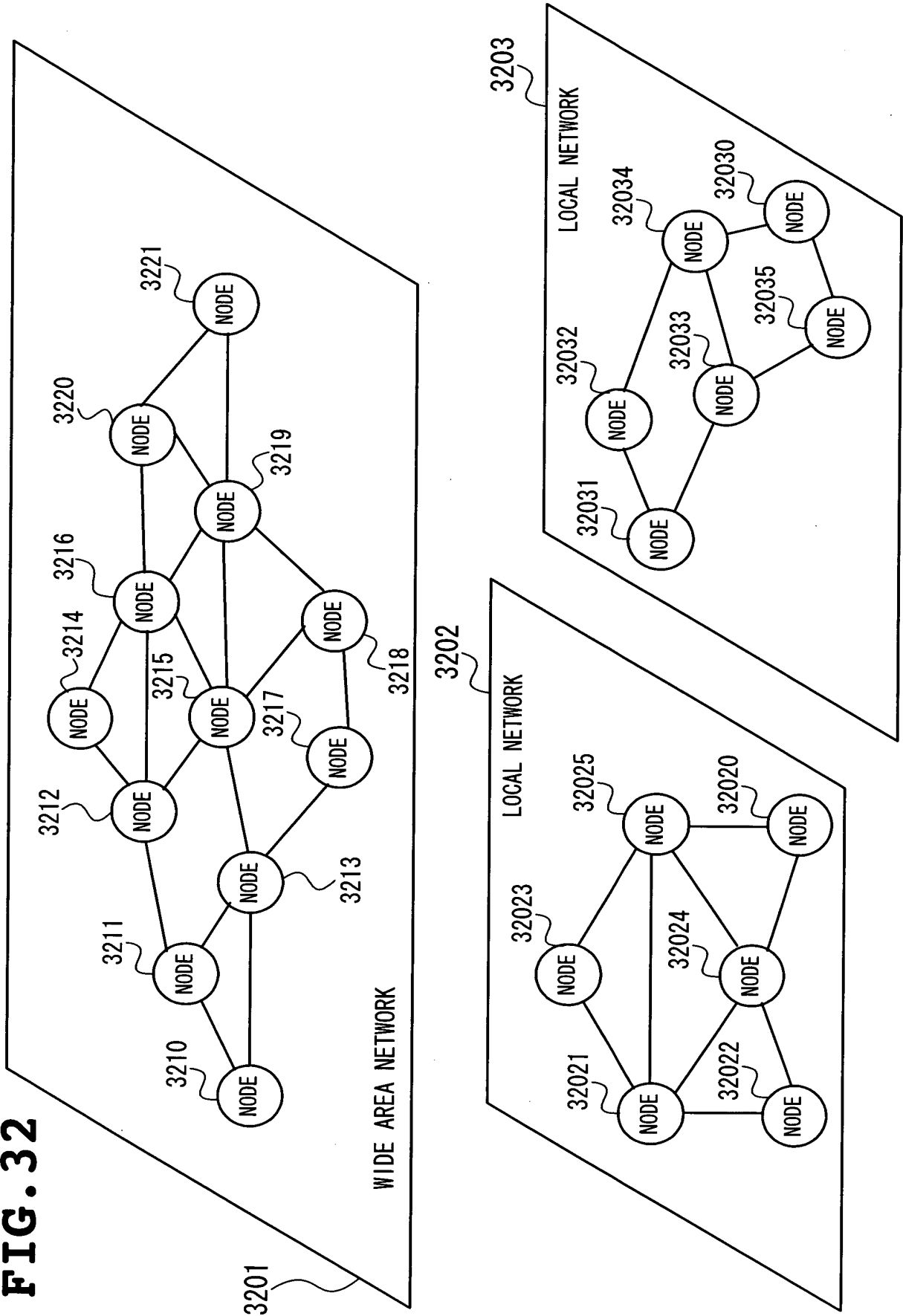


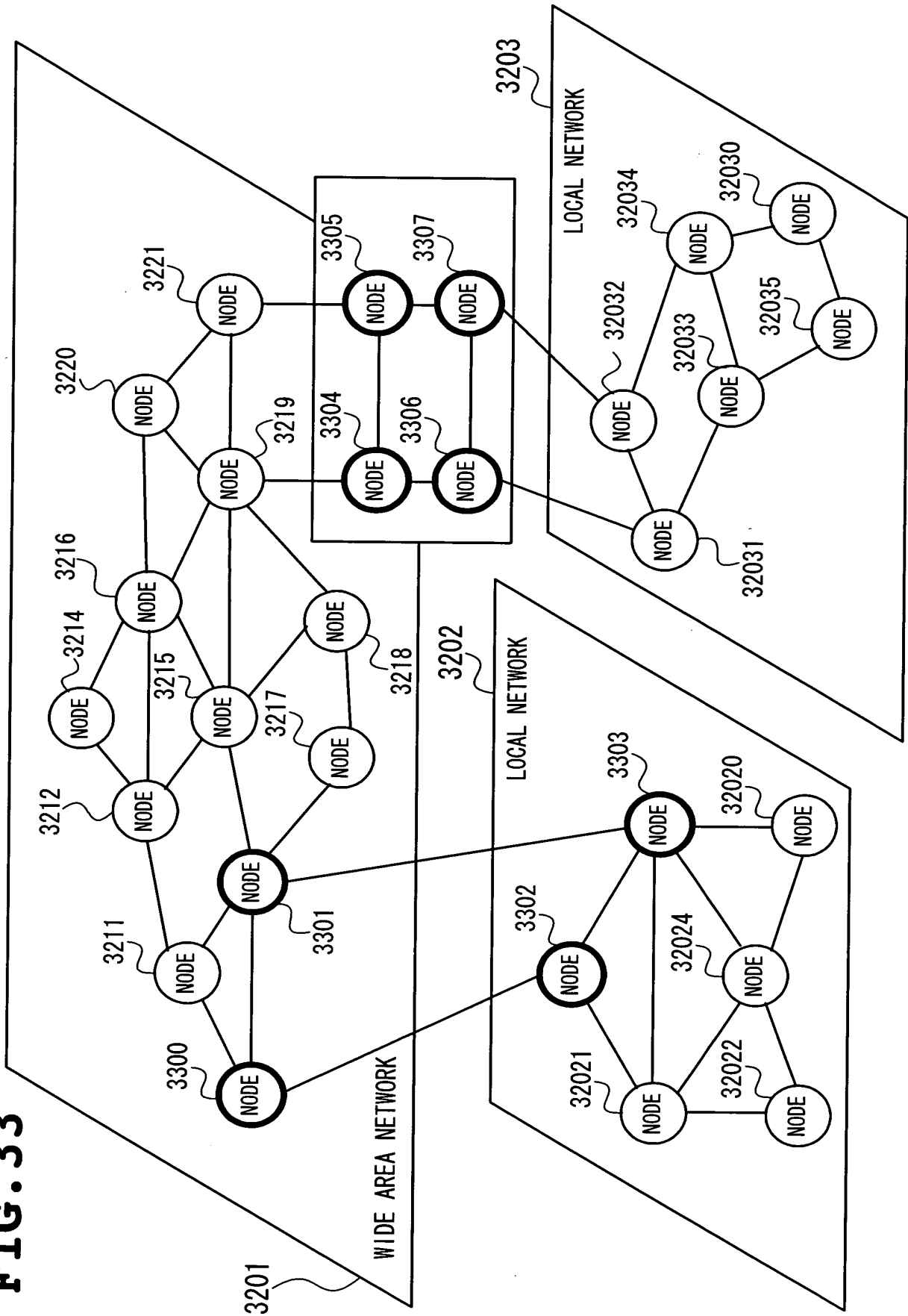
FIG. 33

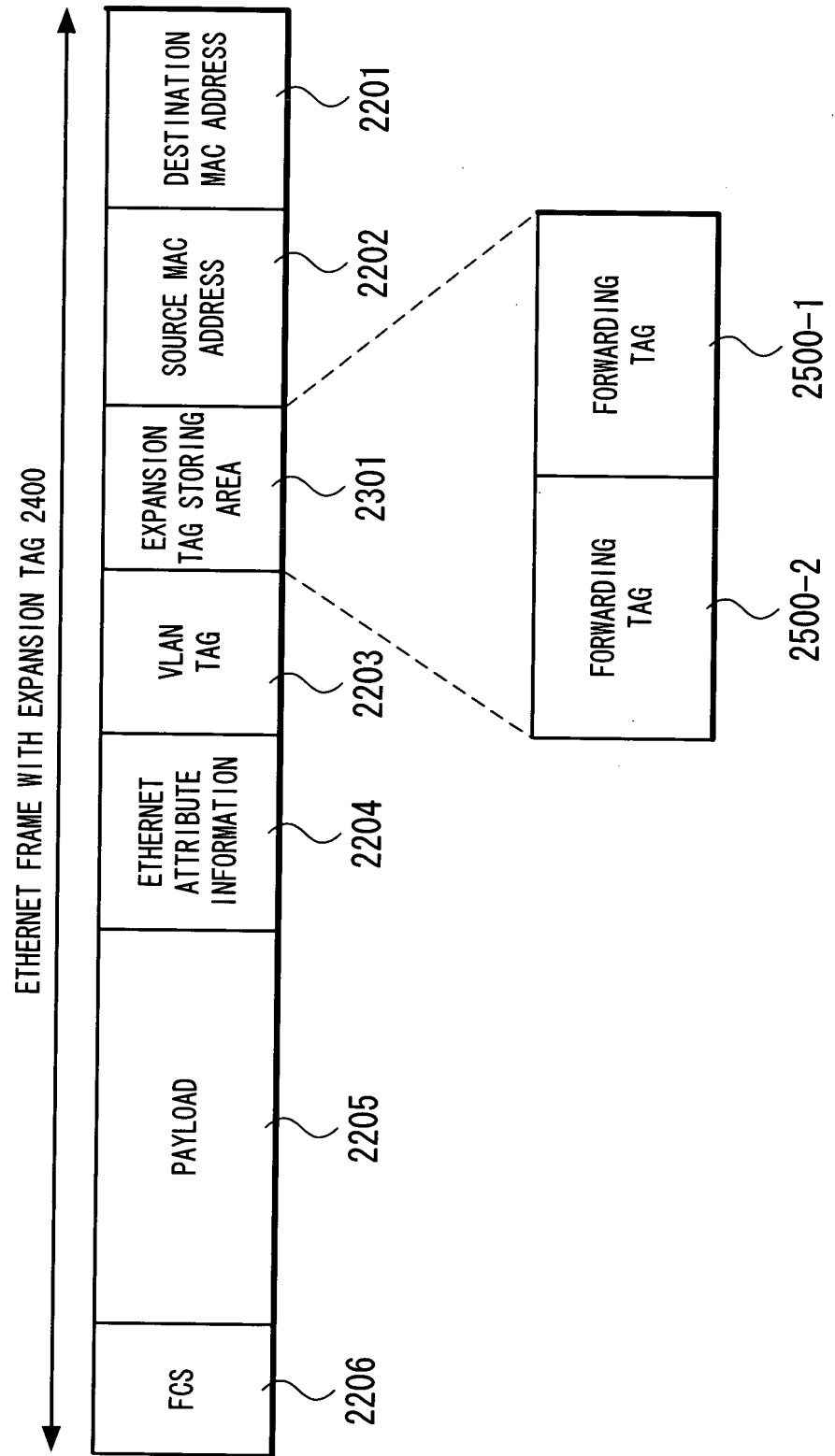
FIG. 34

FIG. 35